1. An integrated circuit chip comprising:

a substrate having semiconductor devices and interconnection lines formed thereover;

a passivation layer overlying said substrate;

a discrete capacitor mounted above said passivation layer; and

one or more wirebonds electrically connected to said discrete capacitor.

2. The integrated circuit according to Claim 1 wherein said discrete capacitor is connected to said one or more wirebonds through said interconnection lines.

3. The integrated circuit according to Claim 1 wherein said one or more wirebonds connect to a contact pad exposed through openings in said passivation layer.

4. The integrated circuit according to Claim 1 wherein said capacitor connects to a contact pad formed in openings in said passivation layer.

5. The integrated circuit according to Claim 1 further comprising a metal line system overlying said passivation layer.

6. The integrated circuit according to Claim 5 wherein said one or more wirebonds are connected to said capacitor through said metal line system.

7. The integrated circuit according to Claim 1 wherein said discrete capacitor is connected to a post-passivation metal line system and wirebonding is also connected to said post-passivation metal line system.

8. The integrated circuit according to Claim 3 wherein said discrete capacitor is connected to a post-passivation metal line system and to said wirebonds.

9. An integrated circuit chip comprising:

a substrate having semiconductor devices and interconnection lines formed thereover;

a passivation layer overlying said substrate;

a discrete capacitor mounted above said passivation layer; and

one or more wirebonds electrically connected to a contact pad formed in openings in said passivation layer.

10. The integrated circuit according to Claim 9 wherein said capacitor connects to a contact pad formed in openings in said passivation layer.

11. The integrated circuit according to Claim 9 further comprising a post-passivation metal line system overlying said passivation layer.

12. The integrated circuit according to Claim 11 wherein said discrete capacitor is connected to said post-passivation metal line system and to said wirebonds.

13. The integrated circuit according to Claim 9 wherein said contact pad comprises an aluminum pad exposed through said openings in said passivation layer.

14. The integrated circuit according to Claim 9 wherein said contact pad comprises a metal cap formed in said opening on an aluminum pad.

15. An integrated circuit comprising:

semiconductor device structures in and on a substrate;

a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein there is at least one contact pad connected to said interconnection lines;

a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

wirebonds formed overlying said passivation layer and connected to said at least one contact pad; and

at least one discrete decoupling capacitor mounted on a solder wettable surface over said passivation layer.

16. The integrated circuit according to Claim 15 wherein said wirebonds comprise gold.

17. The integrated circuit according to Claim 15 wherein said solder wettable surface comprises a printed solder cream.

18. The integrated circuit according to Claim 15 wherein said solder wettable surface comprises solder, copper, or gold.

19. The integrated circuit according to Claim 15 further comprising a diffusion barrier metal layer underlying material having said solder wettable surface.

20. The integrated circuit according to Claim 15 wherein said at least one decoupling capacitor is connected to said wirebonds through said contact pad underlying said passivation layer.

21. The integrated circuit according to Claim 15 wherein said at least one discrete decoupling capacitor is connected to power/ground buses within said substrate.

22. The integrated circuit according to Claim 15 further comprising thick metal lines formed overlying said passivation layer.

23. The integrated circuit according to Claim 22 wherein said thick metal lines are connected to said contact pad through openings in said passivation layer.

24. The integrated circuit according to Claim 22 wherein said at least one decoupling capacitor is connected to said wirebonds through said thick metal lines.

25. The integrated circuit according to Claim 15 wherein said solder wettable surface lies on said thick metal lines.

26. The integrated circuit according to Claim 15 wherein said wirebonds are formed on said contact pad.

27. The integrated circuit according to Claim 15 wherein said wirebonds are formed on said thick metal lines.

28. The integrated circuit according to Claim 15 wherein a gold pad is formed underlying said wirebond.

29. The integrated circuit according to Claim 15 further comprising:

a first post-passivation dielectric layer overlying said passivation layer; and

thick metal lines formed overlying said first post-passivation dielectric layer and connected to said contact pad through openings in said first post-passivation dielectric layer and said passivation layer wherein said at least one decoupling capacitor is connected to said wirebonds through said thick metal lines.

30. The integrated circuit according to Claim 29 wherein said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

31. The integrated circuit according to Claim 29 further comprising a second post-passivation dielectric layer overlying said thick metal lines wherein said at least one decoupling capacitor is connected to said thick metal lines through openings in said second post-passivation dielectric layer.

32. The integrated circuit according to Claim 15 further comprising:

first thick metal lines overlying said passivation layer and connected to said contact pad through openings in said passivation layer;

a first post-passivation dielectric layer overlying said first thick metal lines;

second thick metal lines formed overlying said first post-passivation dielectric layer and connected to said first thick metal lines through openings in said first post-passivation dielectric layer; and

a second post-passivation dielectric layer overlying said second thick metal lines wherein said at least one decoupling capacitor is connected to said wirebonds through said second thick metal lines.

33. The integrated circuit according to Claim 32 wherein said first and second post-passivation dielectric layers comprise polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

34. A method of fabricating an integrated circuit chip comprising:

forming semiconductor device structures in and on a substrate;

forming a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes at least one contact pad;

depositing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

opening first vias through said passivation layer to said at least one contact pad and opening second vias through said passivation layer to said at least one contact pad;

forming wirebonds connected to said at least one contact pad in said first vias;

forming a solder wettable surface on said at least one contact pad in said second vias; and

mounting at least one discrete decoupling capacitor on said solder wettable surface.

35. The method according to Claim 34 wherein said wirebonds comprise gold.

36. The method according to Claim 35 wherein said step of forming said solder wettable surface comprises printing a solder cream on said at least one contact pad.

37. The method according to Claim 35 wherein said step of forming said solder wettable surface comprises electroplating, electroless plating, or sputtering said solder pads with solder, copper, or gold.

38. The method according to Claim 35 further comprising depositing a diffusion barrier metal layer underlying said solder wettable surface and overlying said at least one contact pad.

39. The method according to Claim 35 wherein said at least one discrete decoupling capacitor is connected to wirebonds and to power/ground buses within said substrate.

40. A method of fabricating an integrated circuit chip comprising:

forming semiconductor device structures in and on a substrate;

forming a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes at least one contact pad;

depositing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

forming first thick metal lines overlying said passivation layer and connecting to said at least one contact pad through openings in said passivation layer;

forming wirebonds on said first thick metal lines;

forming a solder wettable surface on said first thick metal lines adjacent to said wirebonds; and

mounting at least one discrete decoupling capacitor on said solder wettable surface.

41. The method according to Claim 39 wherein said wirebonds comprise gold.

42. The method according to Claim 39 wherein said step of forming said solder wettable surface comprises printing a solder cream on said thick metal lines.

43. The method according to Claim 41 wherein said step of forming said solder wettable surface comprises electroplating, electroless plating, or sputtering said thick metal lines with solder, copper, or gold.

44. The method according to Claim 39 further comprising depositing a diffusion barrier metal layer underlying said solder wettable surface and overlying said thick metal lines.

45. The method according to Claim 39 further comprising:

depositing a first post-passivation dielectric layer overlying said passivation layer and underlying said first thick metal lines.

46. The method according to Claim 45 wherein said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

47. The method according to Claim 45 further comprising depositing a second post-passivation dielectric layer overlying said first thick metal lines.

48. The integrated circuit according to Claim 47 wherein said second post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

49. The method according to Claim 39 further comprising:

depositing a first post-passivation dielectric layer overlying said first thick metal lines and wherein said wirebonds and said solder pads are formed through openings in said first post-passivation dielectric layer to said first thick metal lines.

50. The method according to Claim 49 wherein said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

51. The method according to Claim 39 wherein said at least one discrete decoupling capacitor is connected to wirebonds and to power/ground buses within said substrate.

52. A method of fabricating an integrated circuit chip comprising:

forming semiconductor device structures in and on a substrate;

forming a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes at least one contact pad;

depositing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

forming first thick metal lines overlying said passivation layer and connecting to said at least one contact pad through openings in said passivation layer;

depositing a second post-passivation dielectric layer overlying said first thick metal lines;

forming second thick metal lines overlying said second post-passivation dielectric layer and connecting to said first thick metal lines through openings in said second post-passivation dielectric layer;

forming wirebonds on said second thick metal lines;

forming a solder wettable surface on said second thick metal lines adjacent to said wirebonds; and

mounting at least one discrete decoupling capacitor on said solder wettable surface.

53. The integrated circuit according to Claim 52 wherein said first and second post-passivation dielectric layers comprise polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

54. The integrated circuit according to Claim 52 wherein said at least one discrete decoupling capacitor is connected to wirebonds and to power/ground buses within said substrate

55. A method of fabricating an integrated circuit chip comprising:

forming semiconductor device structures in and on a substrate;

forming a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes at least one contact pad;

depositing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

forming first thick metal lines overlying said passivation layer and connecting to said at least one contact pad through openings in said passivation layer;

forming wirebonds on said at least one contact pad;

forming solder pads on said first thick metal lines; and

mounting at least one discrete decoupling capacitor on said solder pads.

56. The method according to Claim 55 wherein said wirebonds comprise gold.

57. The method according to Claim 55 further comprising forming a solder wettable surface on said solder pads.

58 The method according to Claim 57 wherein said step of forming said solder wettable surface comprises printing a solder cream on said solder pads.

59. The method according to Claim 57 wherein said step of forming said solder wettable surface comprises electroplating, electroless plating, or sputtering said solder pads with solder, copper, or gold.

60. The method according to Claim 57 wherein said at least one discrete decoupling capacitor is connected to power/ground buses within said substrate.

61. The method according to Claim 57 further comprising depositing a diffusion barrier metal layer underlying material having said solder wettable surface and overlying said solder pad.

62. The method according to Claim 55 further comprising:

depositing a first post-passivation dielectric layer overlying said passivation layer and underlying said first thick metal lines.

63. The method according to Claim 62 wherein said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.

64. The method according to Claim 62 further comprising depositing a second post-passivation dielectric layer overlying said first thick metal lines.

65. The integrated circuit according to Claim 64 wherein said second post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.